PhD Seminar Talk

Performance and Energy-Efficiency Improvement Techniques for a DRAM based Main Memory

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Even though on-chip caches addressing the memory wall problem are very effective, processor's performance is heavily dependent on main memory. Also, the power consumption of main memory has reached a level where it is almost equal to the processor power, contributing a significant fraction to the overall system power. DRAM has become the ubiquitous solution for memory in all the types of systems (from server to smartphone). Motivated by the internal architecture of the DRAM devices, in this talk we present two techniques that address the performance and power consumption issue of the main memory.

To improve performance, we target the refresh operation and try to reduce its impact on overall system performance. In high-density DRAM devices the amount of time the device spends in refresh is increasing, decreasing the availability of the memory device to the memory controller. We show that with simple modifications to the peripheral circuitry of the DRAM bank, the available parallelism-in-access among different subarrays within a bank can be exploited to reduce the time taken to refresh.

The second technique we present addresses the power consumption in memory. Observing that in a multi-core setup, per memory access the activated page is under utilized, we propose to reduce the page size of the memory. By effectively reducing the number of DRAM cells that are activated per memory request, we significantly reduce the energy consumed during activation and precharge operations. We show that without any disruptive changes to the existing DRAM devices, one can activate half or one-fourth of a page and achieve significant savings in dynamic energy of the memory without any performance loss.

All are welcome